Selected parameters to fit the curve in Fig. 5 are $a_2 = 0.785 \times 10^{-1.5}$ and $b_2 = 1.5$.

The above two curves, (5) and (7), are combined together and expressed by

$$B = (1/1 + aF^{-b}) \tag{8}$$

where the normalized frequency is given by

$$F = (F_1 F_2 / f) \tag{9}$$

and selected values of parameters are $a = 4$ and $b = 1.5$.

As a conclusion, we obtained an approximate dispersion formula:

$$\frac{\beta}{\beta_0} = \frac{\sqrt{\epsilon^*} - \frac{\beta_{TEM}}{\beta_0}}{1 + 4F^{-1.5}} + \frac{\beta_{TEM}}{\beta_0} \tag{10}$$

where

$$F = \frac{4h\sqrt{\epsilon^* - 1}}{\lambda_0}[0.5 + \{1 + 2\log(1 + \frac{W}{h})\}^2]. \tag{11}$$

The estimated values of the propagation constants by the approximate formula (10) and the theoretical values given in Figs. 2 and 3 are compared as a solid line and dots in Fig. 6. The differences between these values were found to be within 1 percent for sampled parameters shown as dots in Fig. 7 in a wide frequency range. The above formula assumes the knowledge of β_{TEM} but a simple formula of β_{TEM} can be easily found in literatures such as Wheeler [8].

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3-GHz 15-W Silicon Bipolar Transistors

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***Abstract*—Silicon bipolar transistors delivering 15-W CW output power with 4.8-dB gain and 38-percent collector efficiency have been developed at 3 GHz. The transistors have been fabricated by boron ion implantation for base region and arsenic diffusion from doped polysilicon for emitter region. Chemical dry-etching techniques for fine patterning and internal-matching techniques have been applied.**

I. Introduction

IN SPITE OF recent progress in power GaAs FET's, silicon bipolar transistors can still be considered the best candidate for solid-state power devices in view of their higher output power and cost performance [1]. Recently the output power capability of silicon bipolar transistors has been extended up to X band and a CW output power of 1.5 W at 10 GHz is reported [2]. However, most efforts are concentrated upon frequencies below 5 GHz and CW output powers of 60 W at 2 GHz and 6 W at 5 GHz are obtained [3]. Although bipolar transistors with 8-W CW output power are commercially available at 3 GHz, further efforts towards increasing CW output power are, to the authors' knowledge, not reported.

On the other hand, the maximum attainable output power is limited not only by the device capability, but also by the device–circuit interface. Hence internal matching procedures are generally used for the improvement of device–circuit interface [4].

This paper reports on recently developed internally matched 3-GHz silicon bipolar power transistors that deliver 15-W CW output power with 4.8-dB gain under class

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C operation. Transistor wafers have been fabricated by using ion implantation, doped polysilicon, and chemical dry-etching (CDE) techniques.

Transistor design, wafer-fabrication processes, internal-matching circuit design considerations, and RF performances are described.

II. Transistor Design

From thermal considerations, a multicell structure is usually adopted in high-power microwave transistors. In our 15-W transistor, tow chips with a total of six cells were operated in parallel, with each cell being capable of giving 3~3.5-W output power. As shown in Fig. 1, the cell was further divided into two subcells with a base bonding pad in common. Each subcell was constructed with an interdigitated emitter–base structure whose effective length and width are ~70 μm and ~260 μm, respectively. The subcell has 28 emitter fingers.

Thermal calculations were performed on junction temperature increase ΔT_j for two 70-μm long and 260-μm wide rectangular planar heat sources on a 90-μm thick silicon wafer (see Fig. 2(a)), as a function of heat source spacing S. In this calculation, the dissipation power of each heat source was taken to be 2.5 W. As shown in Fig. 2(b), ΔT_j for $S \geqslant 90$ μm is calculated to be less than 1.2 times ΔT_j for $S = \infty$. Thus the spacing between two subcells was chosen to be 90 μm. The transistor chip with 2.0×0.5-mm^2 size was composed of three cells.

As shown in Fig. 2(c), the spacing between the cells was chosen to be 370 μm, indicating that ΔT_j is only 5 percent higher than ΔT_j for an infinite cell spacing as seen from Fig. 2(b).

Fig. 3 shows a cross-sectional view of the interdigitated structure. Emitter or base fingers are spaced at a pitch of 9 μm to obtain a 6-dB power gain at 3 GHz. The width of emitter diffusion hole and base contact hole is 1.5 μm, and emitter and base electrode width is 2.5 μm. Thus the spacing between base and emitter electrodes is 2.0 μm. A gold/molybdenum/titanium metal system was adopted to form the metal electrodes. The emitter electrode length was determined to be 60 μm to keep the current density at the root of each emitter finger less 5×10^5 A/cm^2. The molybdenum layer was used not only as a barrier metal but also as an emitter ballasting resistor at the root of each emitter finger.

III. Transistor Fabrication Process

In order to obtain a higher output power by multicell operation, a better uniformity among the cells and a fine patterning have to be realized. To achieve these requirements, the intrinsic base region was formed by an ion-implantation technique.

Boron (B^{11}) ions were implanted into an n-type epitaxial layer through 1000-Å thick SiO_2 layer at an acceleration energy of 40 keV with a dose density of 1.2×10^{14} cm^{-2}, followed by 20-min annealing at 900°C in nitrogen atmosphere.

The emitter region was fabricated by arsenic diffusion from arsenic doped polysilicon, thus reducing emitter–base short-circuit failures. Arsenic and boron concentration profiles were measured using SIMS (Secondary Ion Mass Spectroscopy). The measured results are shown in Fig. 4, from which the diffusion depth and surface concentration of the emitter were found to be 1400 Å and 2×10^{20} cm^{-3}, respectively, and the width and peak concentration of the intrinsic base were found to be 2200 Å and 2×10^{18} cm^{-3}, respectively.

In order to define the fine patterns with a minimum dimension of 1.5-μm reproducibly and uniformly, we employed the CDE technique reported by Horiike *et al.* [5] successfully to etch Si_3N_4, polysilicon and molybdenum layers within ± 0.2-μm accuracy. With mixed gasses of CF_4 and O_2, we chose etching rates of 300 Å/min for Si_3N_4 and 3000 Å/min for polysilicon. The metal electrodes were defined by etching gold, molybdenum, and

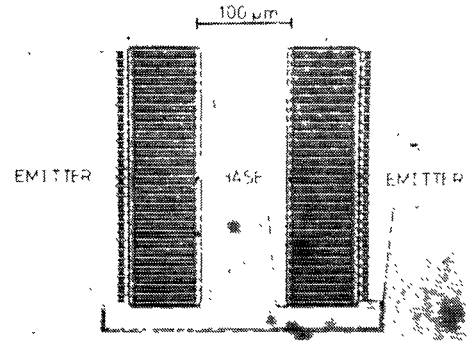

Fig. 1. Top view of a single-cell of transistor.

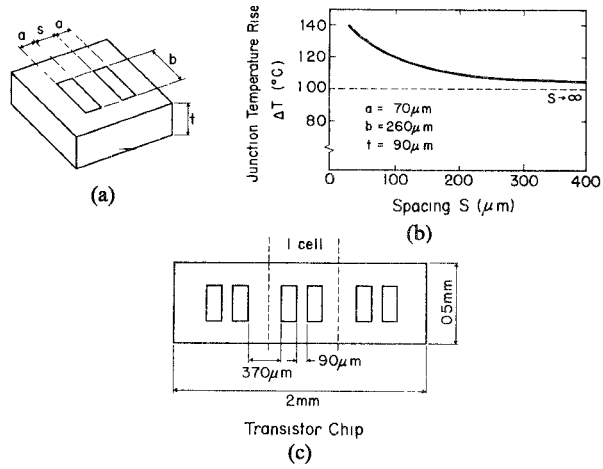

Fig. 2. (a) Heat source model for thermal calculation. (b) Junction temperature rise ΔT_j as a function of heat source spacing S. (c) Configuration of transistor chip.

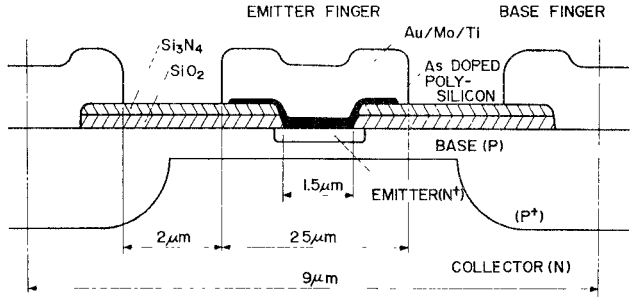

Fig. 3. Cross-sectional view of interdigitated transistor structure.

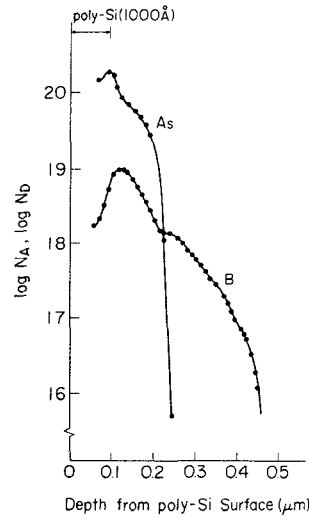

Fig. 4. Arsenic and boron concentration profiles measured by using SIMS.

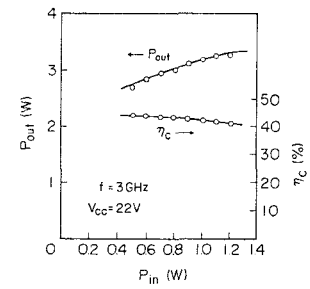

Fig. 5. CW performance of one-cell transistor at 3 GHz.

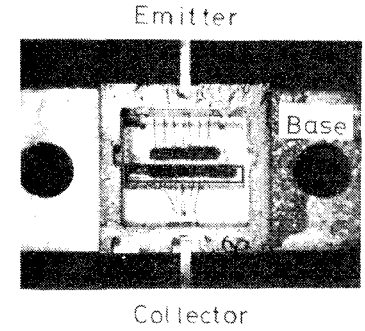

Fig. 6. Inside view of packaged transistor with internal-matching circuit.

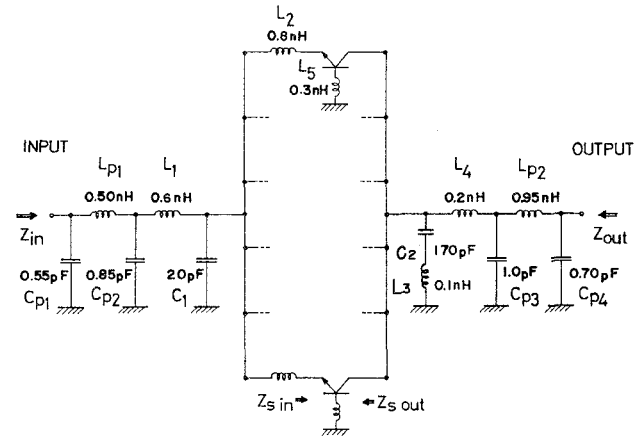

Fig. 7. Equivalent circuit of packaged six-cell transistor with internal-matching network.

titanium successively by sputter etching, CDE, and chemical etching techniques, respectively.

Fig. 5 shows the CW performance of a single-cell transistor. An output power of 3.3 W and a collector efficiency of 43 percent are obtained at an input power of 1 W at collector voltage of 22 V. Transition frequency (or cutoff frequency) f_t and maximum frequency of oscillation f_{max} have been estimated to be 3.6 GHz and 7 GHz, respectively, by measuring small-signal scattering parameters of a common-emitter single-cell transistor. These agree well with theoretically estimated f_t of 3.7 GHz corresponding to a base width of 2200 Å and f_{max} of 8.7 GHz, given by

$$f_{max} = \frac{f_t}{8\pi R_{bb'} C_c}$$

where

$$R_{bb'} = 0.44\ \Omega$$

and

$$C_c = 4.8\ \text{pF}.$$

IV. Internal-Matching Circuit Design

In today's high-power microwave transistors, the internal-matching technique is commonly used to improve device–circuit interface difficulties. We also employed the internal-matching technique in our six-cell transistor as shown in Fig. 6. The outer size of the package ceramics is 10×10 mm^2. The equivalent circuit of the transistor is shown in Fig. 7, where $\{C_{p1}, L_{p1}, C_{p2}\}$ and $\{C_{p3}, L_{p2}, C_{p4}\}$ approximately represent the package parasitics of the emitter and collector port, respectively. The values of the package parasitics, given in Fig. 7, were first calculated from the physical dimensions of the package and then slightly modified to account for the measured impedances of empty and shorted packages measured over 2–4 GHz.

Before determining the optimum values of C_1, C_2, L_1, L_2, L_3, and L_4, input and output impedances $Z_{s\ in}$ and $Z_{s\ out}$ of a single cell at conjugate match conditions were measured by using a substitution method for a package-mounted single-cell transistor without internal matching circuitry, which was operated at collector voltage of 22 V with output power of 3.3 W for input power of 1 W. After subtracting the impedances due to the package parasitics and bonding wires, $Z_{s\ in}$ and $Z_{s\ out}$ including the base grounding inductance were found to be $2.5 + j4\ \Omega$ and $3.0 + j8\ \Omega$, respectively.

Using $Z_{s\ in}$ and $Z_{s\ out}$ and the equivalent circuit of package parasitics, input and output matching networks $(L_1, C_1, L_2, L_3, L_4, C_2)$ for the six-cell transistor were determined as given in Fig. 7. L_2 is the inductance of the bonding wires connecting the emitters of each transistor cell to the MOS capacitor indicated by C_1. L_1 represents the bonding wires between C_1 and the thick-film line on an alumina frame of the package.

The values of L_1, C_1, and L_2 were first determined by a computer optimization with respect to the input VSWR, and further modification for L_2's was performed to realize better uniform operation among the cells taking into account the mutual inductance between L_2's of six cells. The values of L_2's for the outer cells have been made by a factor of $\sim$1.2 times longer than those of the inner cells.

The output-matching circuit consists of shunt inductance of the bonding wires resonating in parallel with the effective transistor output capacitance C_c at the frequency of interest. The shunt inductance L_3 corresponds to the bonding wires from the ground plane of the package to the bypass capacitors C_2 which were mounted at each end of the transistor chip mounting area. L_4 represents the bonding wires connecting the collector to the output transmission line of the package.

The input and output impedance Z_{in} and Z_{out} of six-cell transistor were measured to be $8.2+j32.5\ \Omega$ and $7.5+j33.2\ \Omega$, respectively, at 3 GHz. These values agree fairly well with the calculated values of Z_{in} and Z_{out} of $8.1+j9.4\ \Omega$ and $8.7+j29\ \Omega$, respectively, which are obtained by using the single-cell impedance $Z_{s\,in}$ and $Z_{s\,out}$ and internal-matching elements values shown in Fig. 7. Due to dimensional limitation of the package, Z_{in} and Z_{out} could not be brought to near 50 Ω.

V. RF Performance

RF performance of the six-cell transistor operated under class C were measured using a microstrip circuit with external input and output matching networks. Fig. 8 shows output power (P_{out}), gain, collector efficiency (η_c), and input VSWR versus input power (P_{in}) characteristics at 3 GHz and collector voltage of 22 V. A maximum output power of 15.8 W has been obtained at an input power of 6 W with collector efficiency of 37 percent. At 5-W input power, 15-W output power has been obtained with 4.6-dB gain and 38-percent collector efficiency.

Measured P_{out} and η_c versus P_{in} characteristics are shown in Fig. 9 for one-, two-, four-, and six-cell transistors. The curves for the six-cell transistor are the same ones as in Fig. 8. Output powers (input powers) and collector efficiencies of the four-, two-, and one-cell transistors are 12.3 W (4 W)-36 percent, 6.8 W (2 W)-39 percent, and 3.3 W (1 W)-43 percent, respectively. The four-cell transistor is internally matched at input and output ports, and the two-cell transistor is internally matched only at input port.

Fig. 10 shows output power per cell as a function of the number of cells, where we can see the output power per cell decreases with the increment of cell number. This degradation may be due to an increase of unbalanced operation among cells and also due to an increase of matching circuit loss associated with lowering of input and output impedance of transistor chips. Power combining efficiency of the six-cell transistor is found to be 83 percent from Fig. 10.

Junction temperature T_j of the transistor under CW operation has been measured by using an infrared scanner

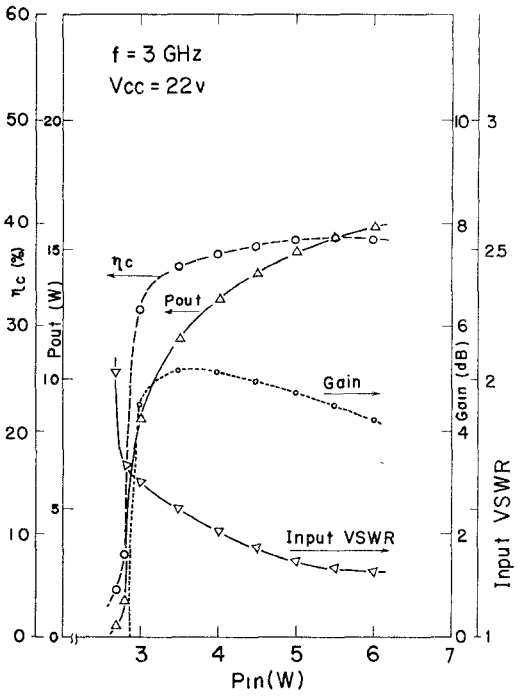

Fig. 8. CW performance of six-cell transistor at 3 GHz.

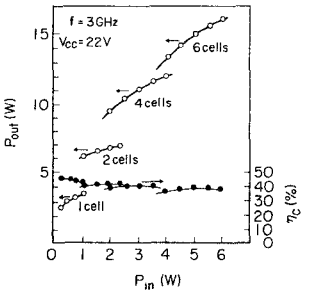

Fig. 9. CW performance of multicell transistors at 3 GHz.

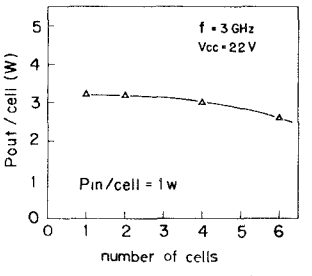

Fig. 10. Output power per cell as a function of number of cells.

(AGA, type 680 thermovision). The peak junction temperature of the one-cell transistor operating at 3.3-W output power with 1-W input power is 145°C and the corresponding thermal resistance is calculated to be 20.4°C/W. Fig. 11 shows the surface temperature distribution of a six-cell transistor operating at an output power of 15 W with input power of 5 W. It can be seen that T_j is larger for the outer cells, and the maximum value of T_j is 153°C for the utmost right cell. The thermal resistance is calculated to be 3.9°C/W.

The observed distribution of T_j among the cells can be considered to arise from the electrical and physical asym-

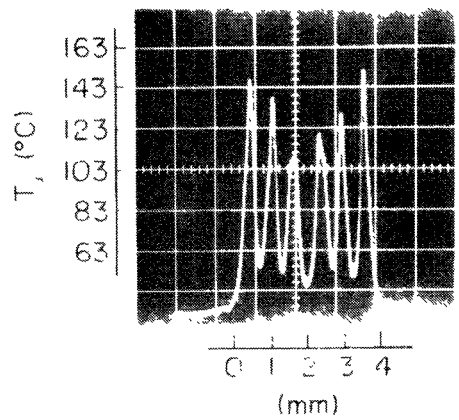

Fig. 11. Junction temperature distribution of six-cell transistor.

metries among the cells. First, twelve emitter bonding wires, 35 μm in diameter and each spaced by 300-μm apart, have mutual inductance. Thus the effective values of L_2's in Fig. 7 are different among the cells. Second, the shunt-matching circuit element L_3 and C_2 are located at both ends of the two transistor chips. Hence, the electrical length will be different among the cells.

In order to estimate the reliability of the developed transistor, accelerated life tests by dc burn-in were performed. An MTTF (Mean-Time-To-Failure) of the six-cell transistor operating at a junction temperature of 153°C can be estimated to be greater than 10^6 h at room temperature.

VI. Conclusion

It has been shown that the developed silicon bipolar transistors can deliver an output power of 15 W at 3 GHz with a gain of 4.8 dB and collector efficiency of 38 percent using six cells. Owing to insufficient internal matching due to the present package restriction, the amplification bandwidth of the six-cell transistor is now limited to ~100 MHz at 3 GHz. In order to broaden the bandwidth, the package improvement is undertaken. It is the authors' belief that, with further advancements of device fabrication and device–circuit interface techniques, the silicon bipolar transistor can still be the best candidate for microwave power devices below ~4 GHz.

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